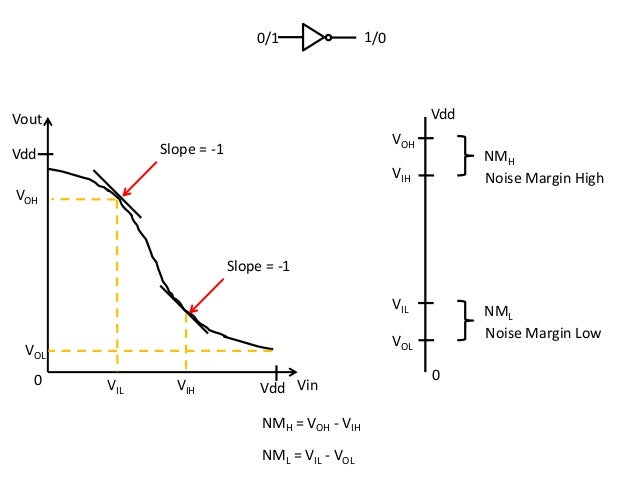
Experiment 2

Aim: To perform the parametric sweep analysis on resistive load inverter to plot VTC Curve for different values of the load resistance and calculate the various critical parameter of VTC Curve for each case.

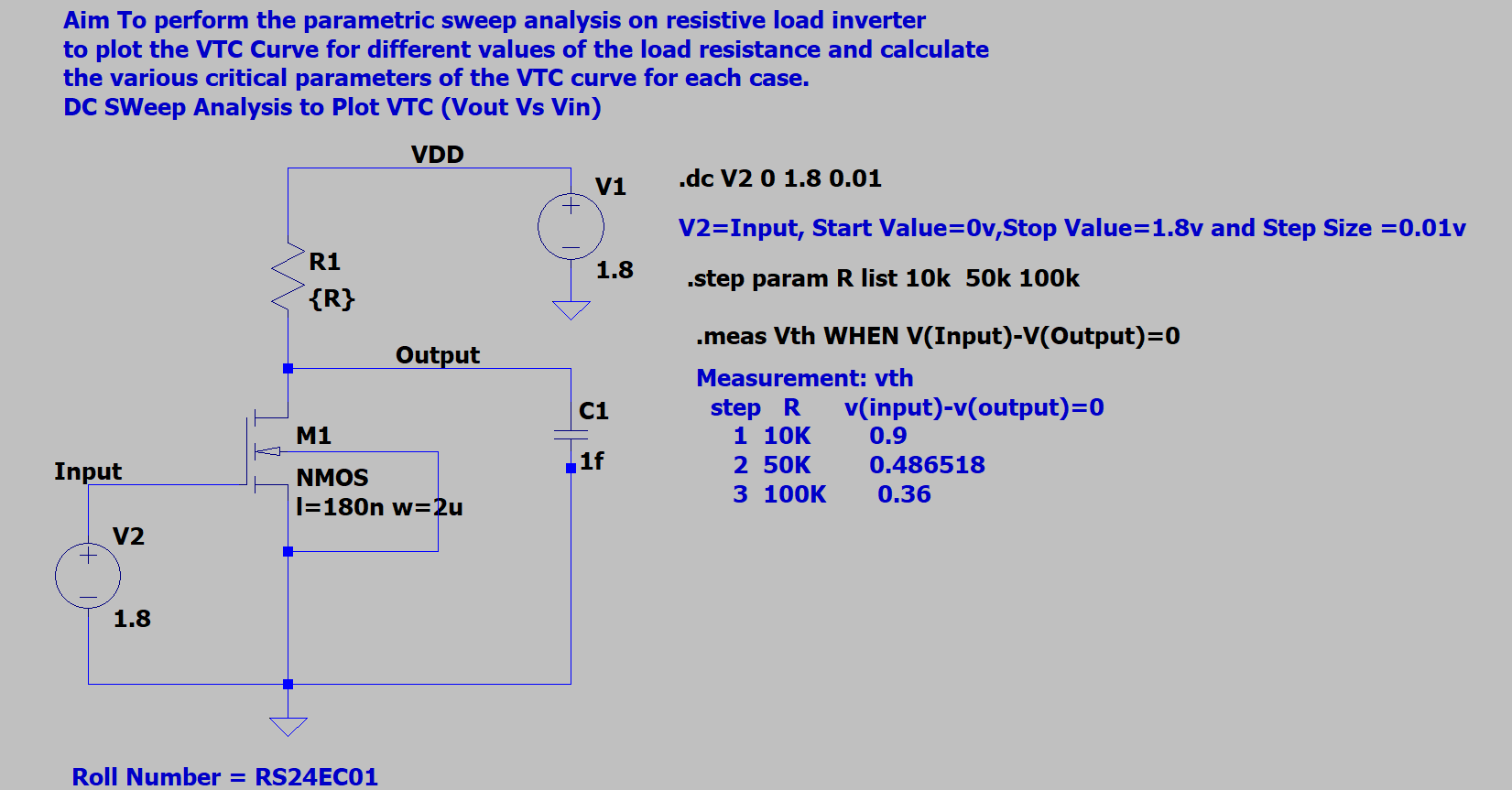
Tool Used: LTSPICE

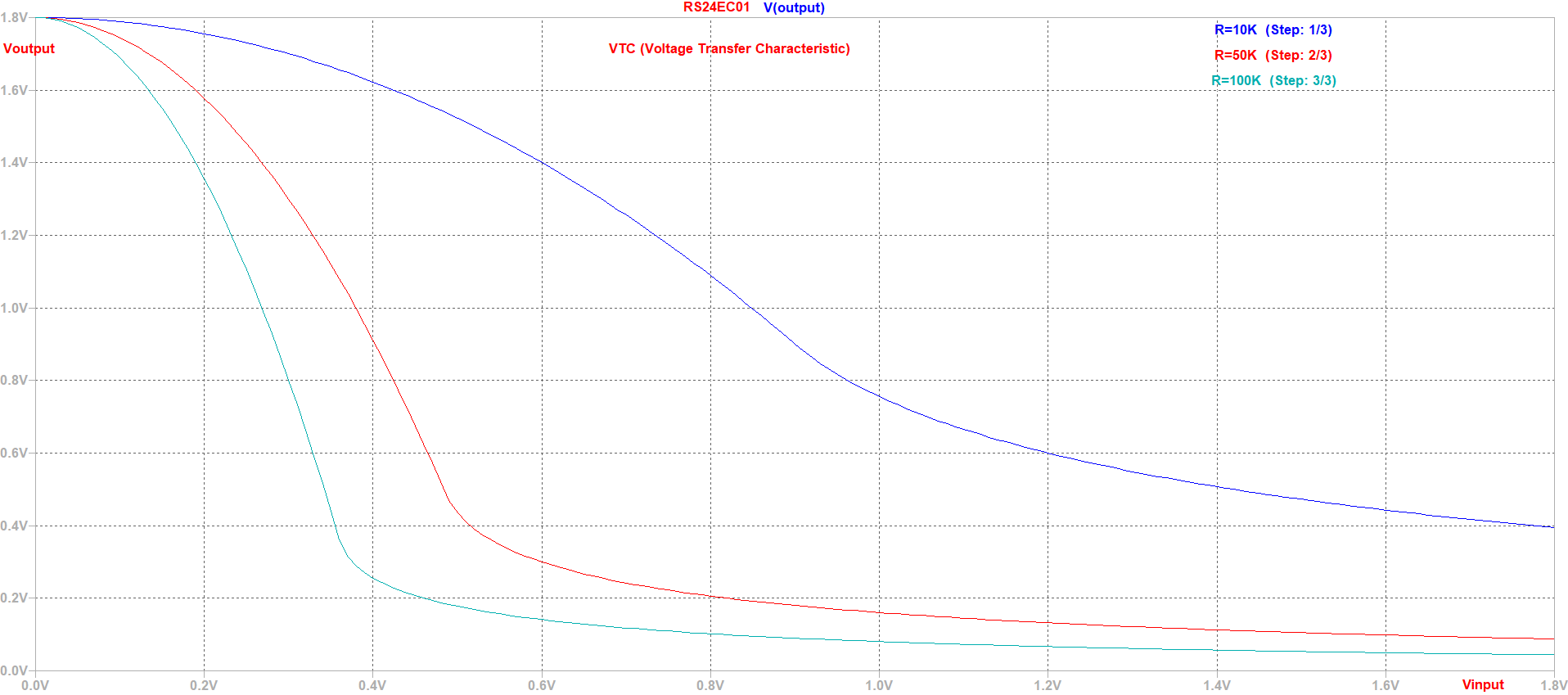
Theory

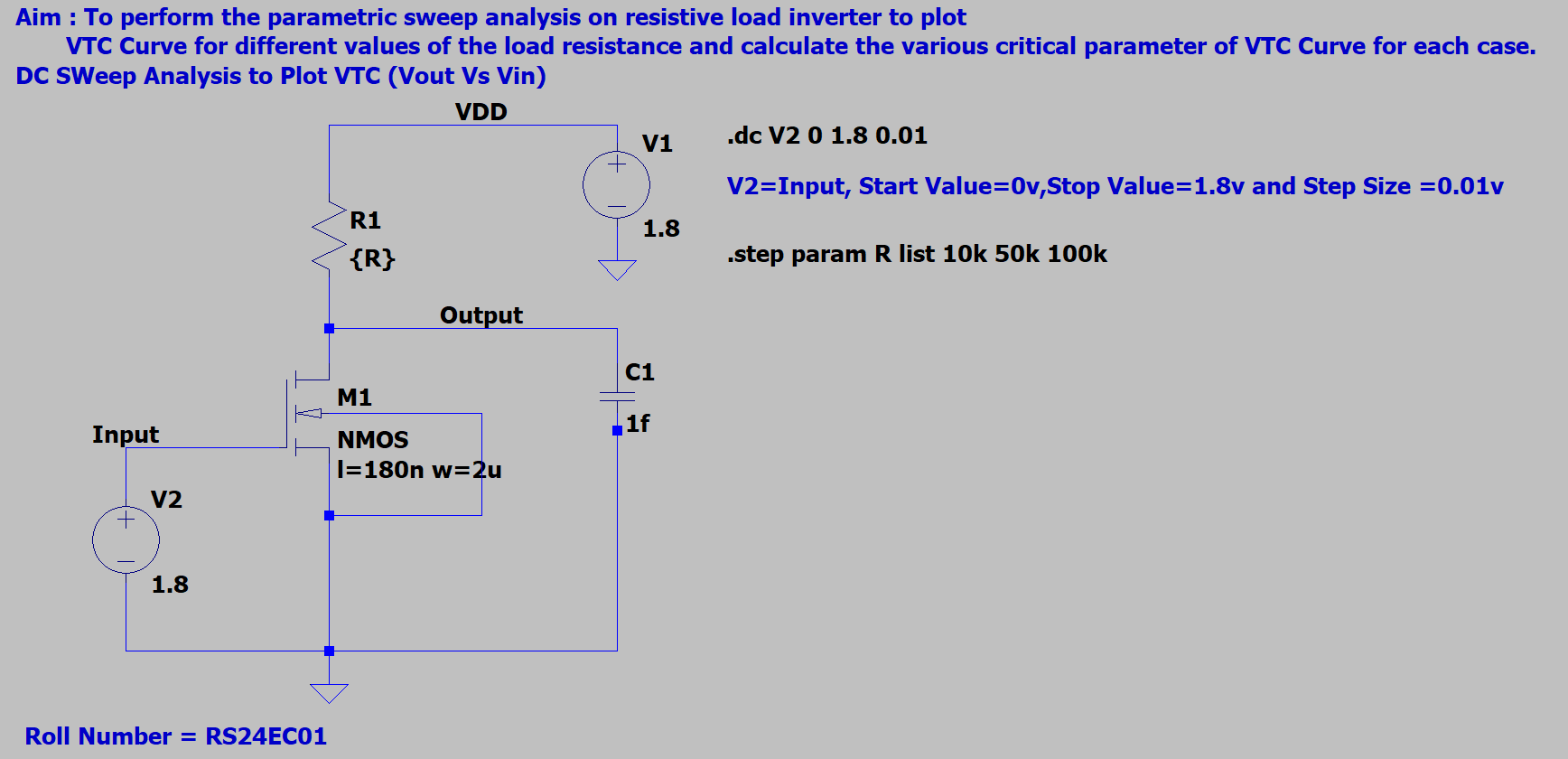
|  |  |
| --- | --- |
| VIL | Input Low Voltage |
|  | Any voltage between 0 and VIL treated as Logic Zero |
| VOH | Output High Voltage |
|  | Any output voltage level between VOH and VDD treated as Logic One |
| VIH | Input High Voltage |
|  | Any Input voltage level between VIH and VDD will be treated as Logic One |
| VOL | Output Low Voltage |
|  | Any output voltage level between Zero and VOL treated as Logic Zero |

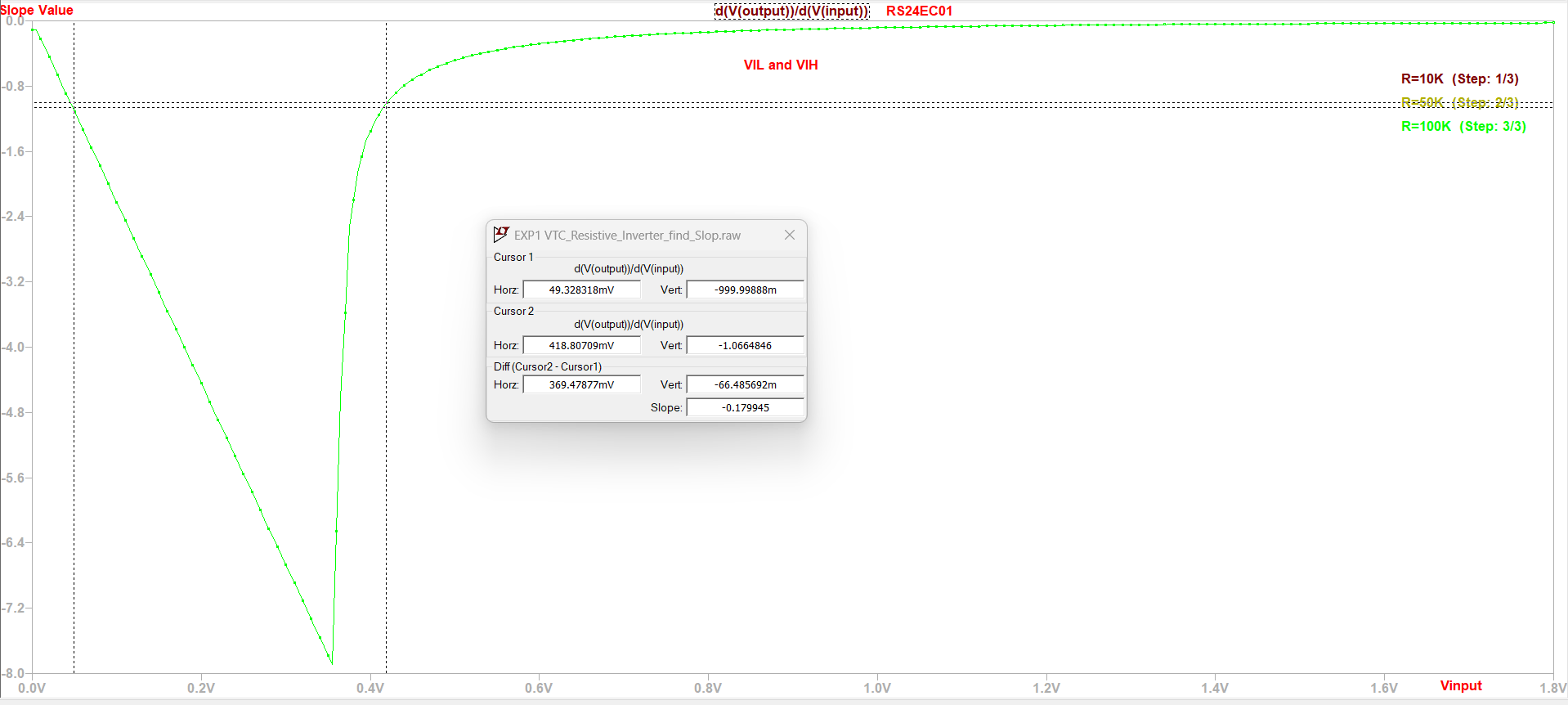


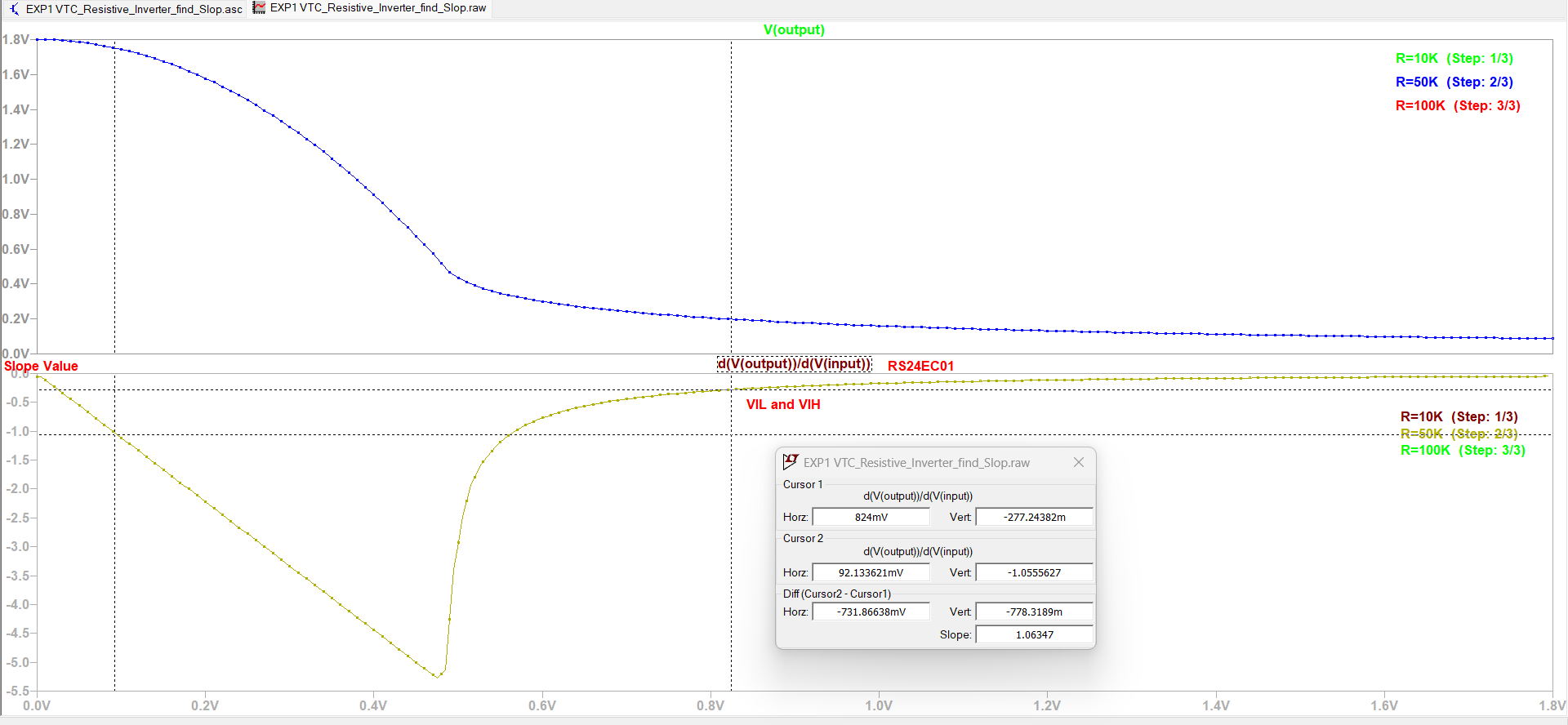
Switching Threshold: A point at which Vin = Vout at this point PMOS and NMOS both are in saturation state both transistors are on. High chances of leakage current flow.

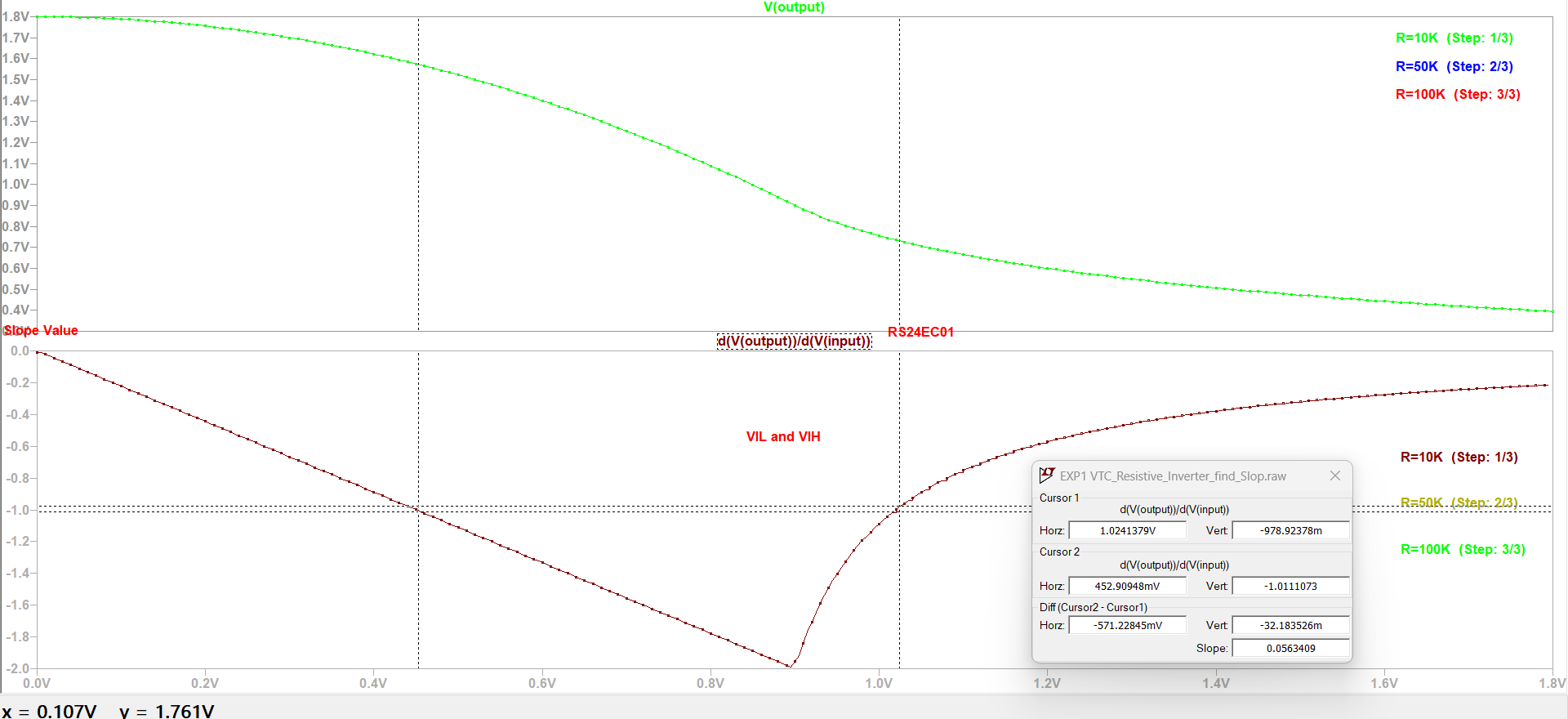
Simulation

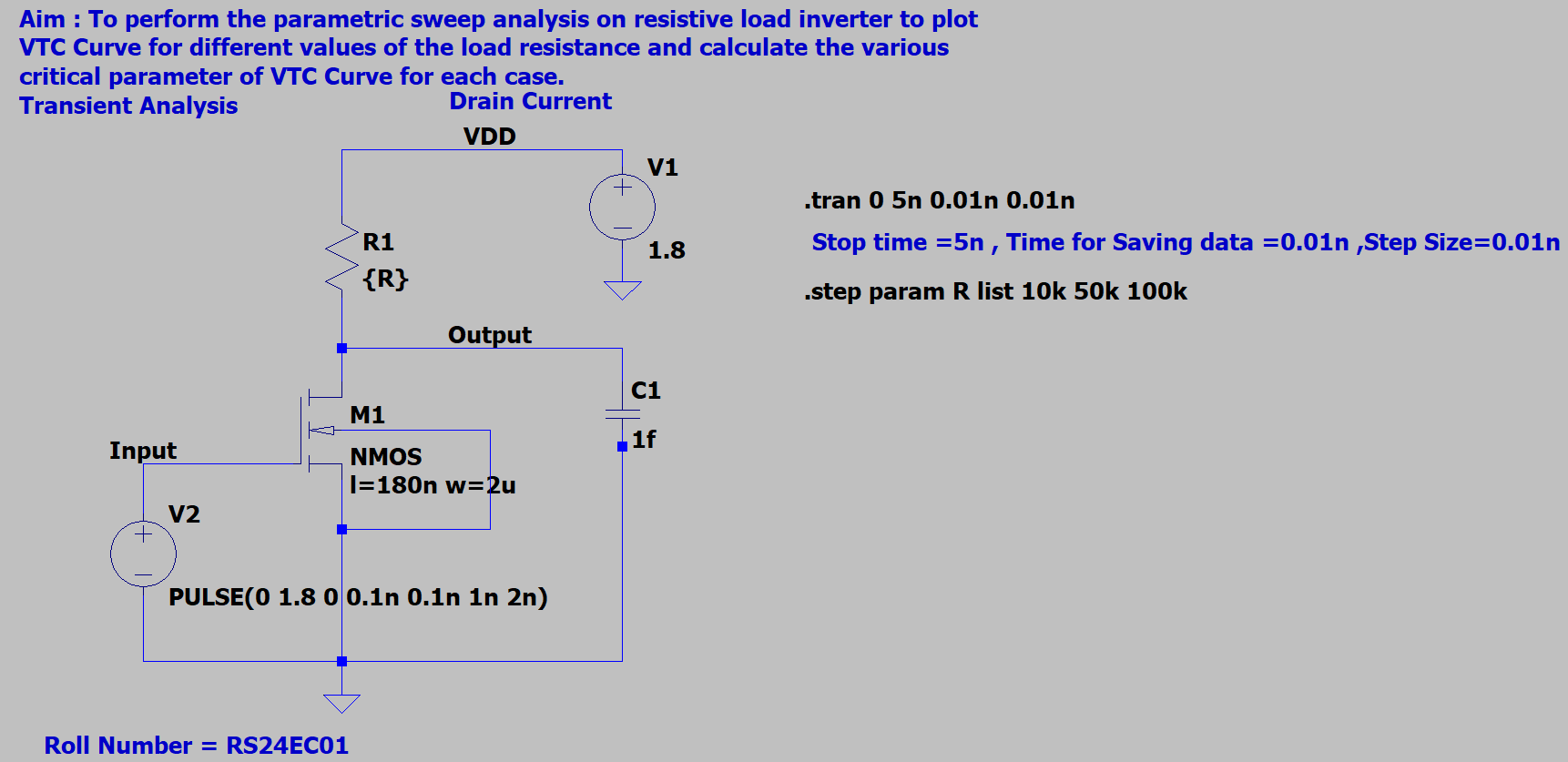


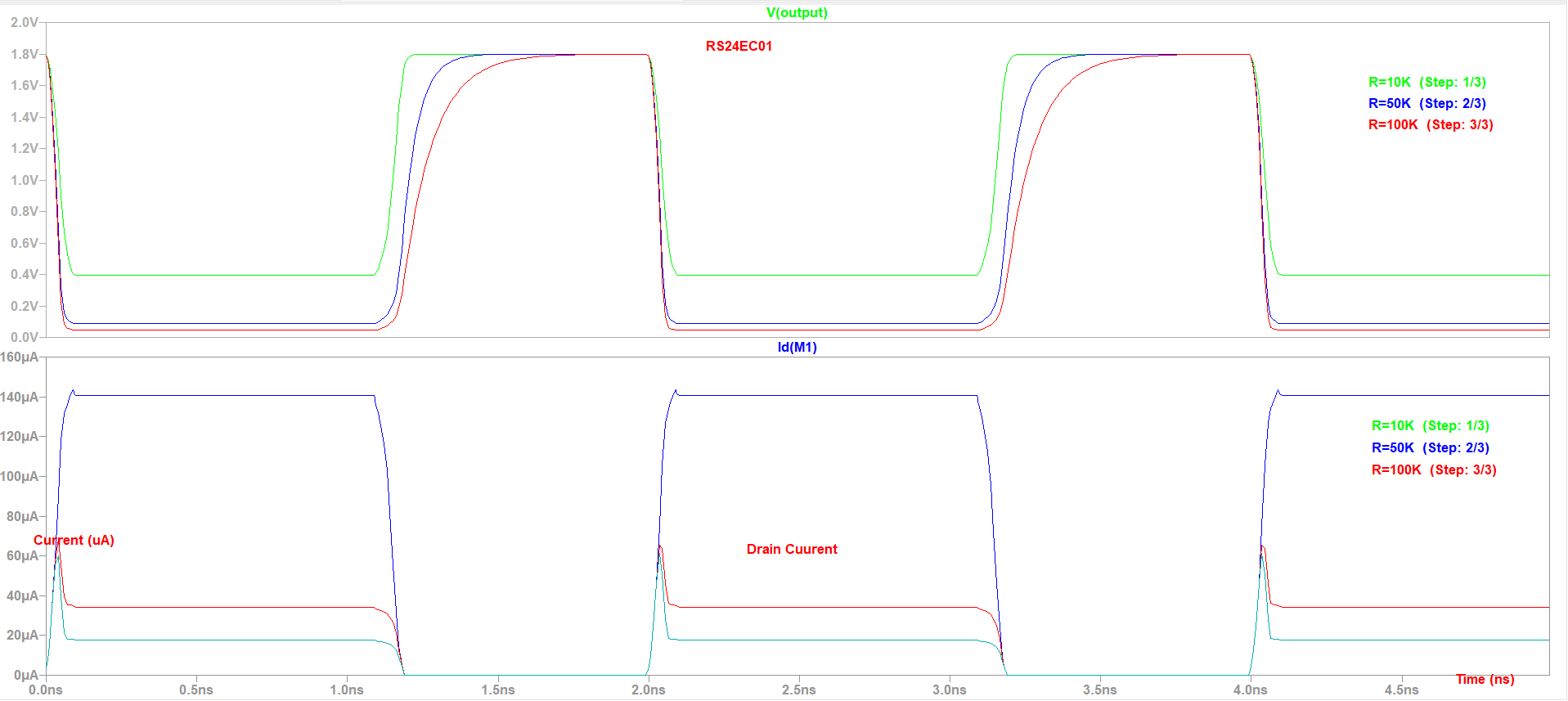


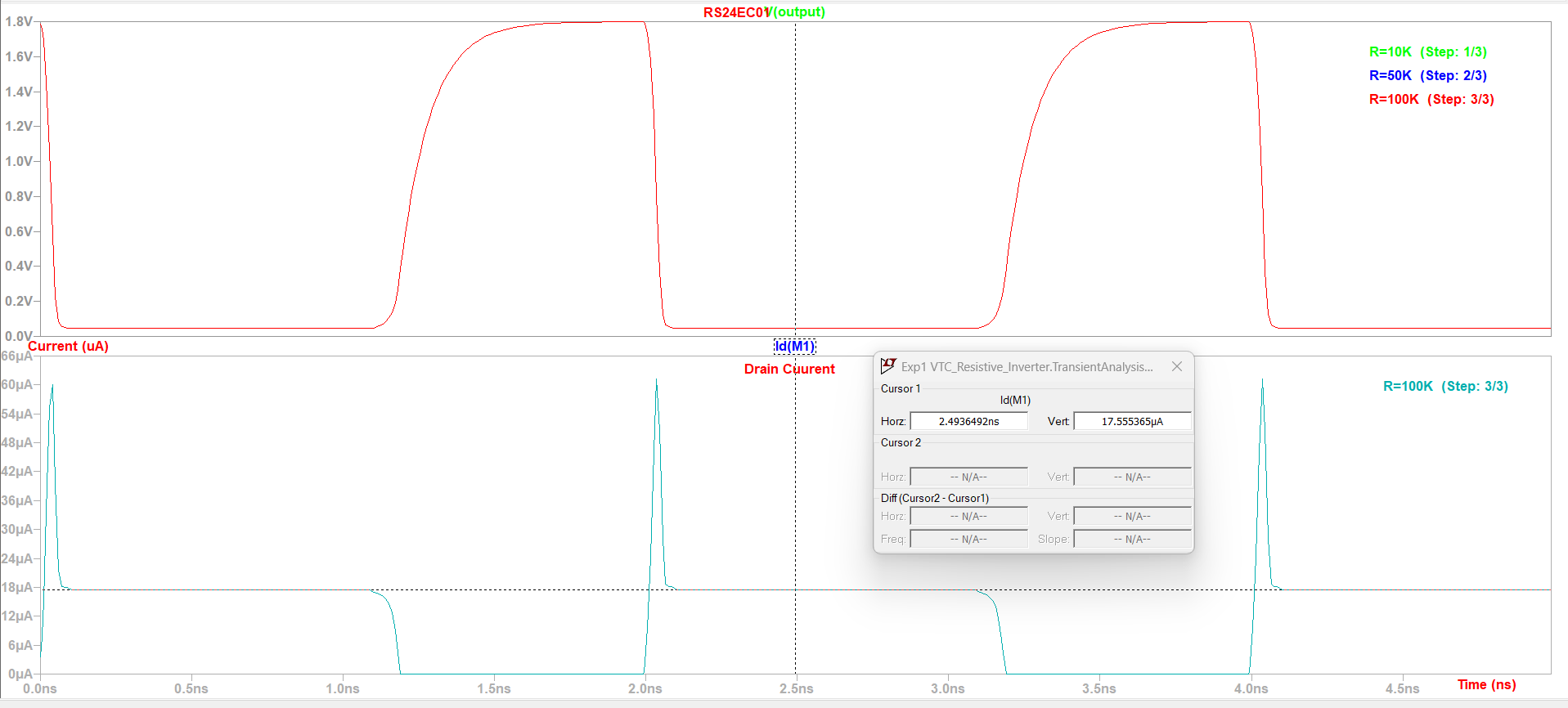


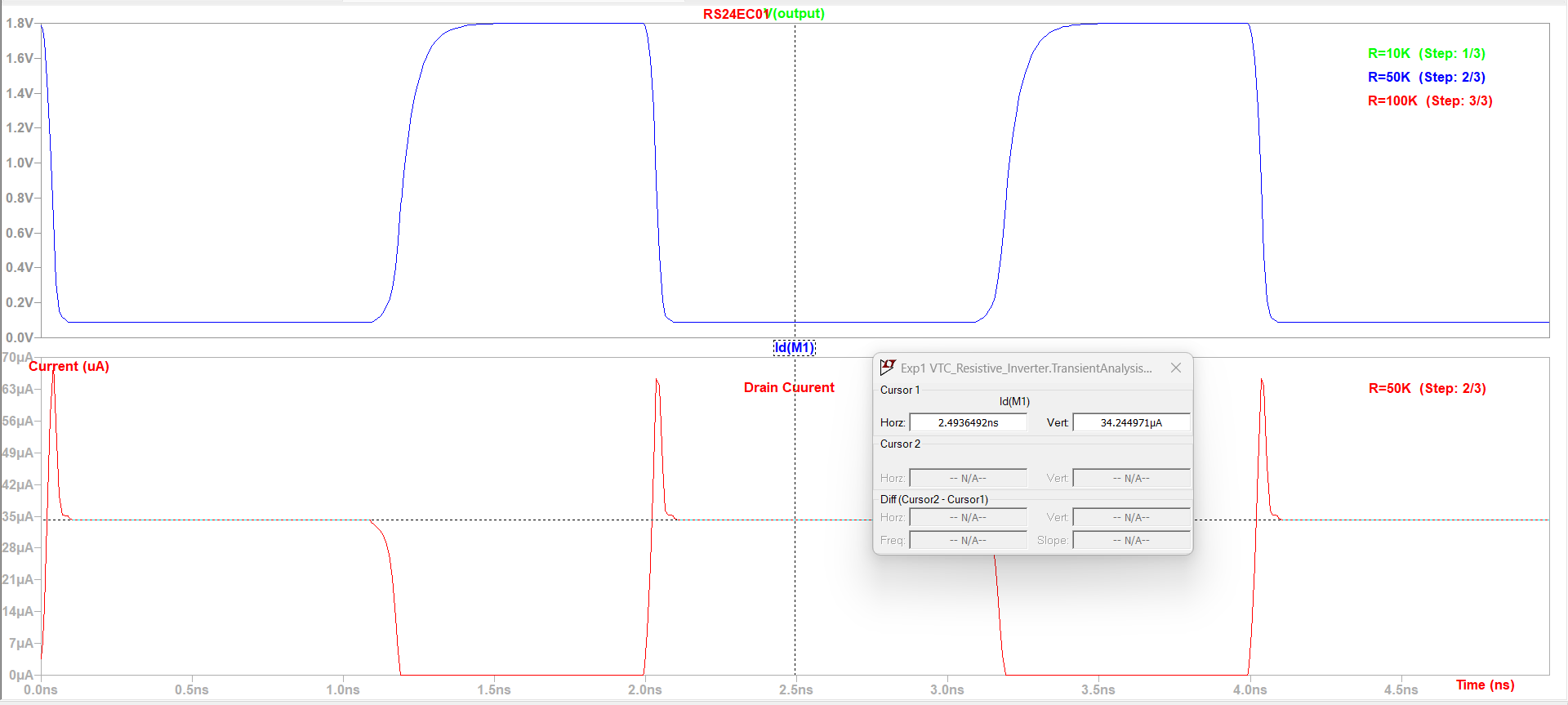


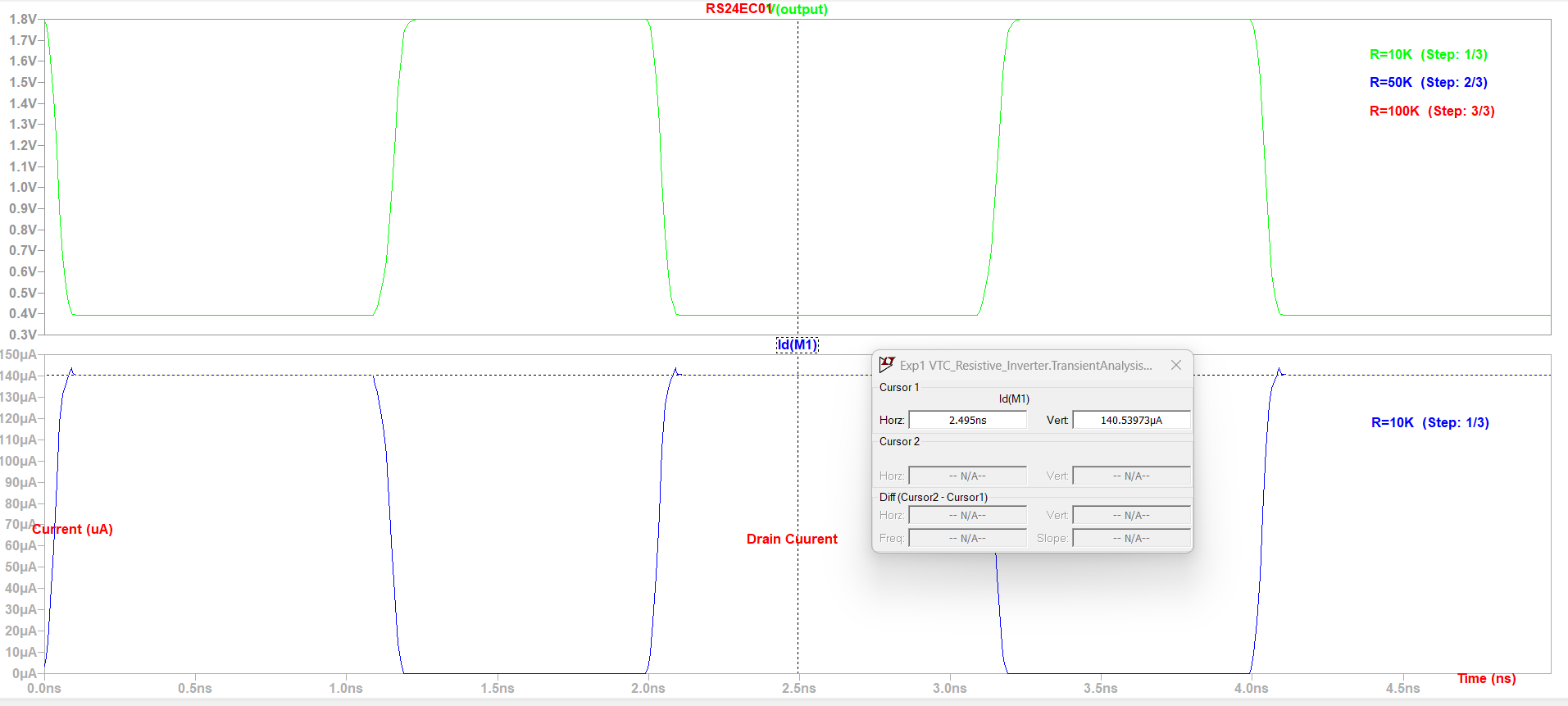


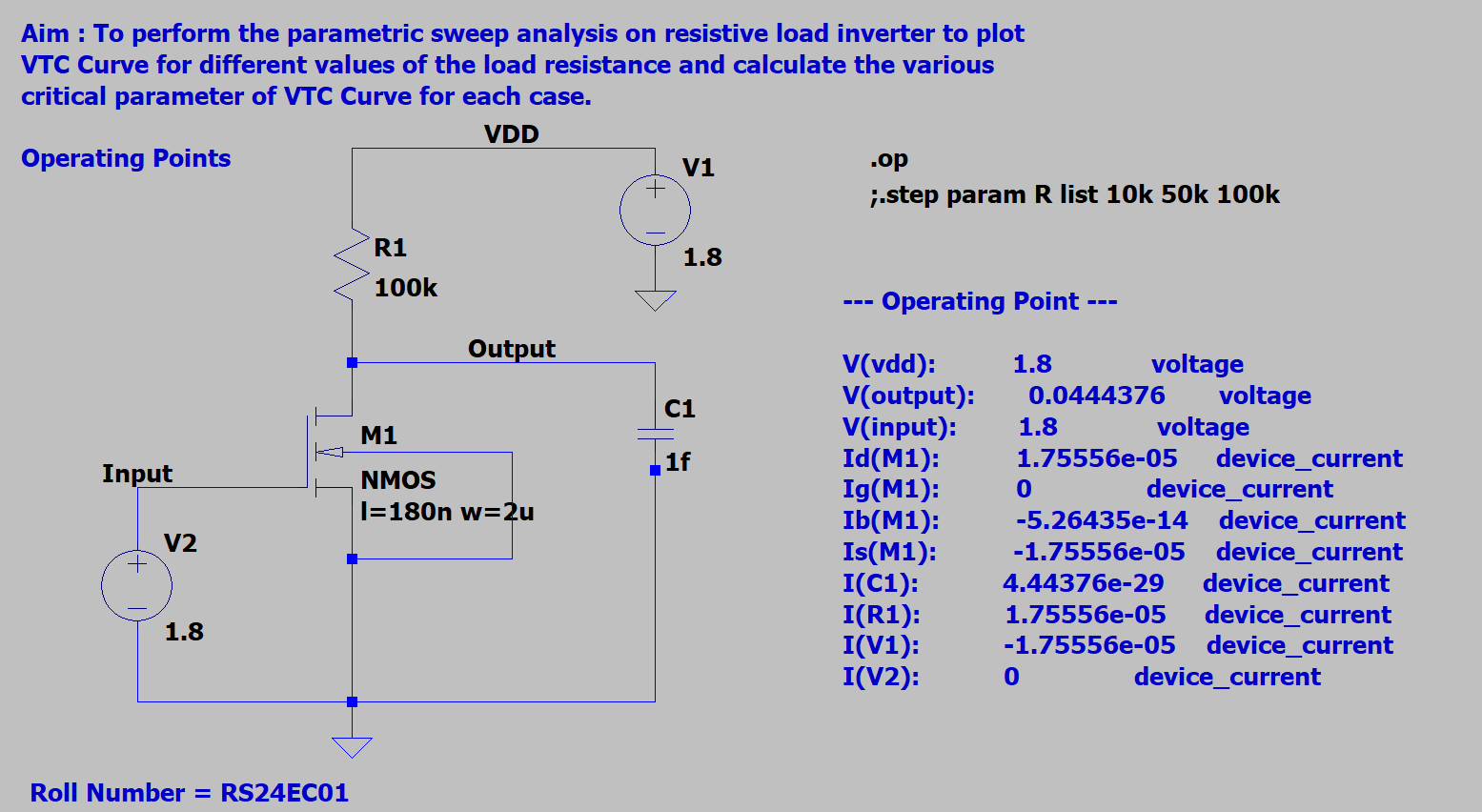


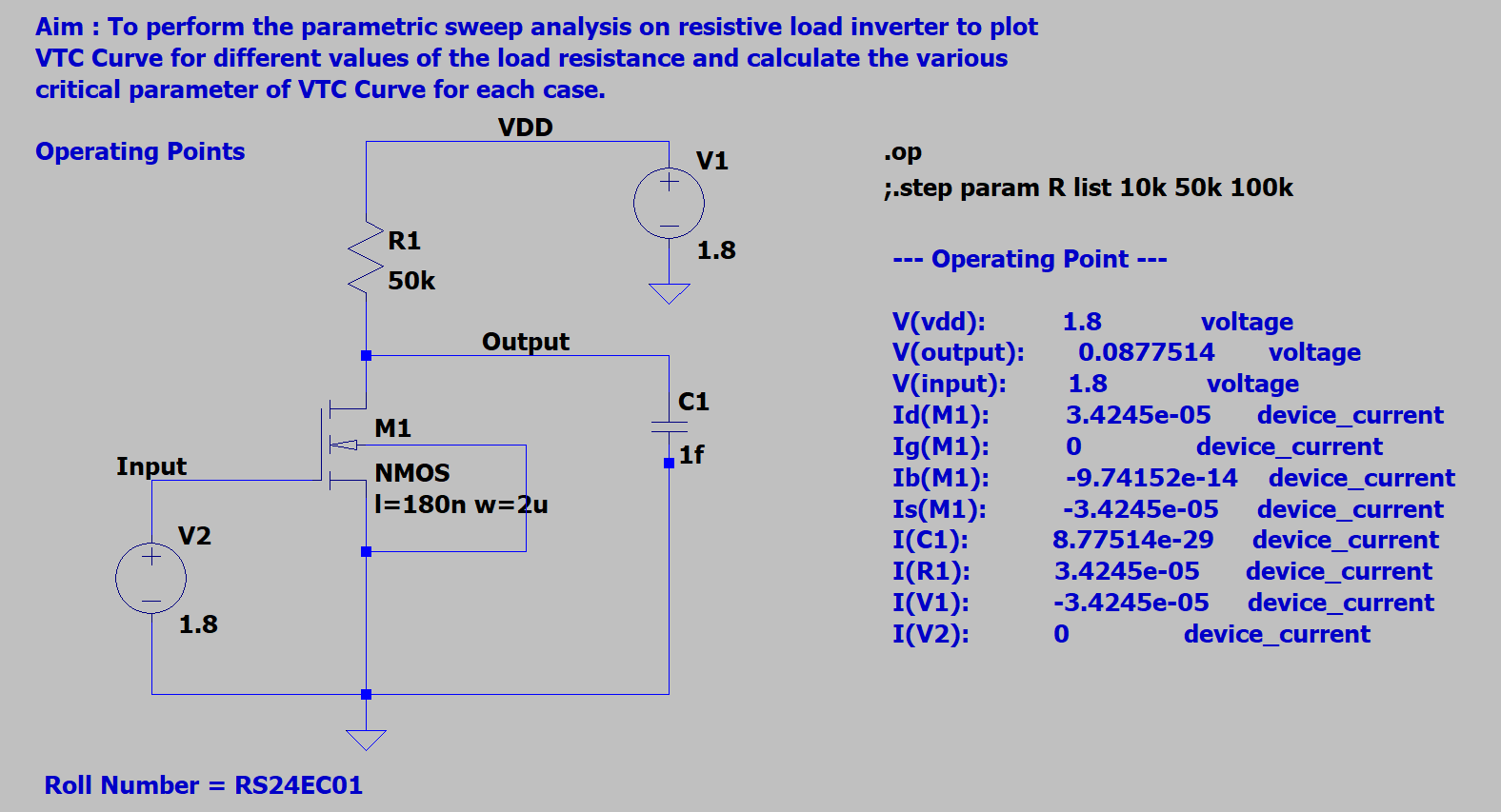


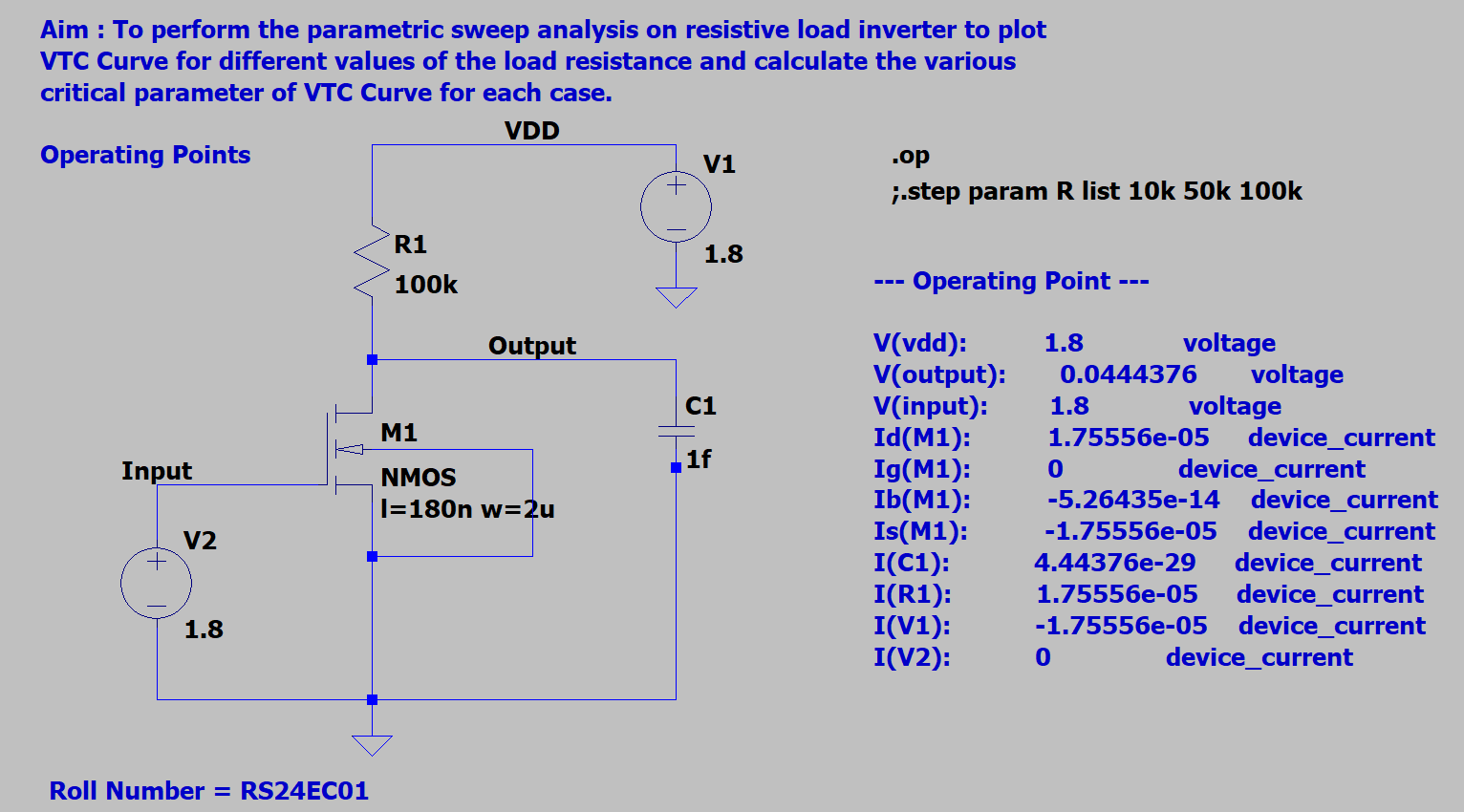


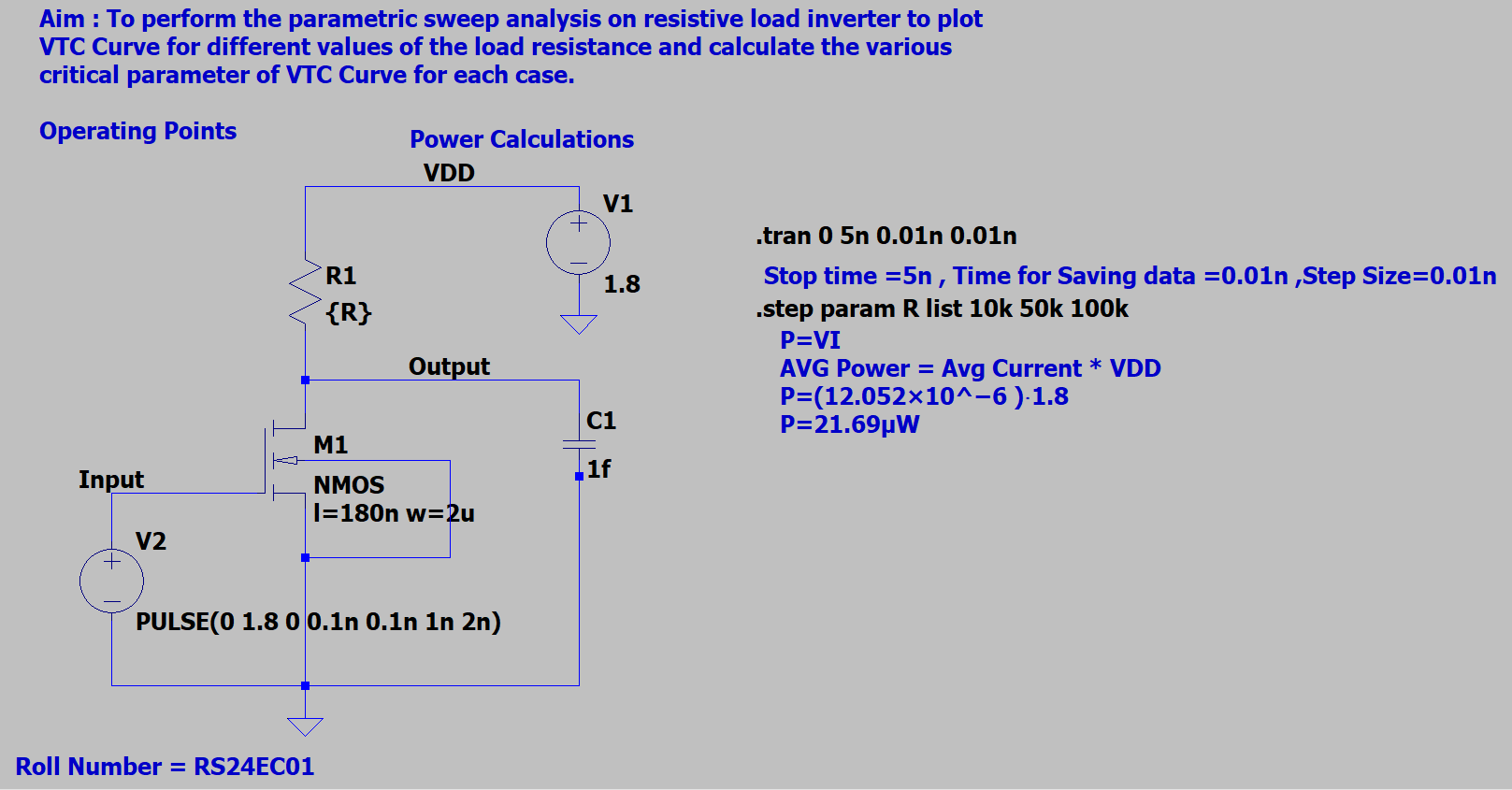


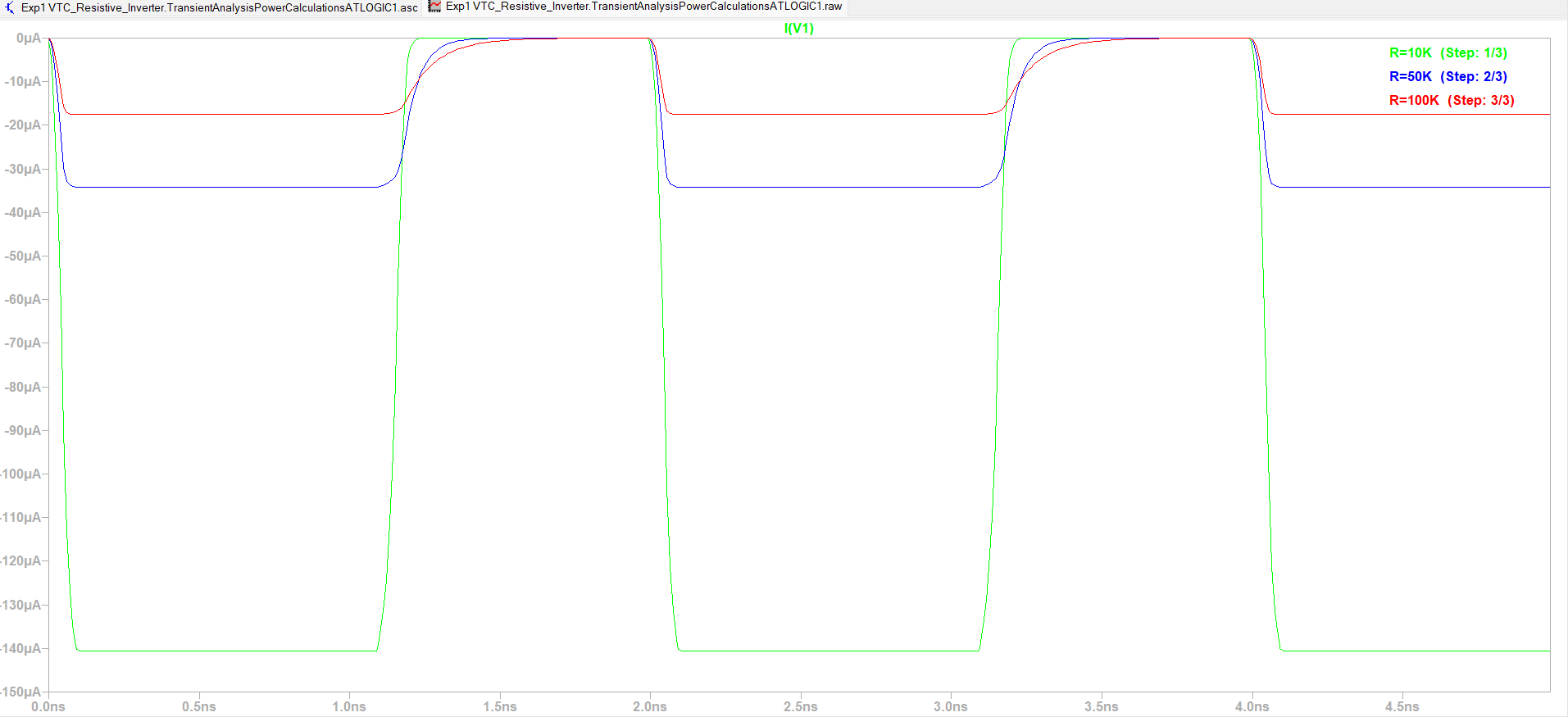












Results

|  |  |
| --- | --- |
| **Parameters** | **Value in mv** |
| **R=100K** |  |
| VIL | 49.328318mV |
| VIH | 418.80709mV |
| VOL | 44.485728mV |
| VOH | 1.8v |
| Vm | 0.36v |
| Transient Analysis |  |
| Id | 17.555365µA |
| Power Calculation |  |
| Avg Current | 12.052µA |
| Avg Power | 12.052µA \* 1.8V |
| **R=50K** |  |
| VIL | 92.133621mV |
| VIH | 565.40948mV |
| VOL | 87.846385mV |
| VOH | 1.8V |
| Vm | 0.486v |
| Transient Analysis |  |
| Id | 34.244971µA |
| Power Calculation |  |
| Avg Current | 22.727µA |
| Avg Power | 22.727µA\*1.8V |
| **R=10K** |  |
| VIL | 452.90948mV |
| VIH | 1.0144397V |
| VOL | 396.88669mV |
| VOH | 1.8V |
| Vm | 0.9v |
| Transient Analysis |  |
| Id | 140.53973µA |
| Power Calculation |  |
| Avg Current | 89.23µA |
| Avg Power | 89.23µA\*1.8V |